

## Asst. Prof. SALİH BAYAR

### Personal Information

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### International Researcher IDs

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Yoksis Researcher ID: 264886

### Biography

Salih Bayar received his BS degree in electronics and communication engineering from Yıldız Technical University, Istanbul, Turkey, in 2003. He has received his MS degree in Electrical Engineering and Information Technology in specialization Systems Engineering from Karlsruhe Institute of Technology, Karlsruhe, Germany, in 2007. During this period, he held various positions at KIT, TEMO Soft-, Hardware & Consulting e.K., Molex and Daimler Chrysler AG. He was a research assistant in the Department of Computer Engineering at Bogazici University, Istanbul, Turkey, between 2007 and 2013. He received his PhD degree from the Department of Computer Engineering at Bogazici University. He worked as a Research and Development Engineer and Manager from 2013 to 2017 in a leading software company, Istanbul, Turkey. Since 2017 he has been an Assistant Professor in the Electrical and Electronics Department at Marmara University, Istanbul, Turkey. His main research interests are parallel computing, distributed systems, reconfigurable computing, dynamic and partial reconfiguration of Xilinx FPGAs, multi-processor and embedded multi-core architectures.

### Education Information

Doctorate, Bogazici University, Institute Of Science, Bilgisayar Mühendisliği (Dr), Turkey 2007 - 2015

Postgraduate, Universitaet Fridericiana zu Karlsruhe, Electrical and Computer Engineering, Department of Electrical Engineering and Information Technology, Germany 2004 - 2007

Undergraduate, Yildiz Technical University, Faculty Of Electrical & Electronics, Electronics And Communication Engineering, Turkey 1998 - 2003

### Foreign Languages

English, C2 Mastery

German, C2 Mastery

### Dissertations

Doctorate, Reconfigurable network-on-chip (NoC) architectures for embedded systems, Boğaziçi Üniversitesi, Fen

Bilimleri Enstitüsü, Bilgisayar Mühendisliği (Dr), 2015

Postgraduate, Implementation, testing and evaluation of methods to reduce power dissipation using dynamic and partial reconfiguration on Xilinx Spartan-III FPGAs, Karlsruhe Institute of Technology, Institute for Information Processing Technology, Electrical Engineering and Information Technology, 2007

## Research Areas

Computer Sciences, Distributed Systems, Parallel Algorithms, Sorting and Searching, Equipment, Processor Architectures, Logic Design, Engineering and Technology

## Academic Titles / Tasks

Assistant Professor, Marmara University, Faculty of Engineering, Electrical and Electronics Engineering, 2017 - Continues

Lecturer, Istanbul Kultur University, Faculty Of Engineering, Department Of Computer Engineering, 2012 - 2013

Lecturer, Beykent University, Faculty Of Engineering-Architecture, Department Of Computer Engineering, 2010 - 2011

## Advising Theses

Bayar S., An area-efficient FPGA implementation of lane and obstacle detection for driving assistance systems, Postgraduate, F.TAT(Student), 2022

Bayar S., Comparison of FPGA design methods through implementation of spatial image filters, Postgraduate, Z.NUR(Student), 2022

Bayar S., Performance evaluation of a parallel image enhancement technique for dark images on multithreaded CPU and GPU architectures, Postgraduate, B.HANGÜN(Student), 2021

Bayar S., Distributed acoustic sensor acquired signals: detection, processing, classification, and parallel implementation, Postgraduate, B.ALLA(Student), 2021

Bayar S., Medical image processing on xilinx FPGAs, Postgraduate, S.SAĞLAM(Student), 2020

## Published journal articles indexed by SCI, SSCI, and AHCI

- I. **Recent advances in Machine Learning based Advanced Driver Assistance System applications**  
Tatar G., Bayar S., Cicek I., Niar S.  
MICROPROCESSORS AND MICROSYSTEMS, vol.100, no.100, pp.1000-1039, 2024 (SCI-Expanded)
- II. **Energy efficiency assessment in advanced driver assistance systems with real-time image processing on custom Xilinx DPU**  
Bayar S., Tatar G.  
JOURNAL OF REAL-TIME IMAGE PROCESSING, vol.21, no.5, pp.157, 2024 (SCI-Expanded)
- III. **An OpenMP-based parallel implementation of image enhancement technique for dark images**  
Hangun B., BAYAR S.  
Signal, Image and Video Processing, vol.18, no.5, pp.4115-4130, 2024 (SCI-Expanded)
- IV. **Hardware Design of Lightweight Binary Classification Algorithms for Small-Size Images on FPGA**  
Saglam S., Bayar S.  
IEEE ACCESS, vol.12, pp.57225-57235, 2024 (SCI-Expanded)
- V. **Real-Time Multi-Learning Deep Neural Network on an MPSoC-FPGA for Intelligent Vehicles: Harnessing Hardware Acceleration With Pipeline**  
Tatar G., Bayar S., Çiçek I.  
IEEE Transactions on Intelligent Vehicles, vol.10, no.4, pp.1-12, 2024 (SCI-Expanded)
- VI. **Real-Time Multi-Task ADAS Implementation on Reconfigurable Heterogeneous MPSoC Architecture**

Tatar G., BAYAR S.

IEEE Access, vol.11, pp.80741-80760, 2023 (SCI-Expanded)

VII. **Parallel implementation of distributed acoustic sensor acquired signals: detection, processing, and classification**

Bencharif B. A. E., BAYAR S., Ozkan E.

JOURNAL OF APPLIED REMOTE SENSING, vol.16, no.2, 2022 (SCI-Expanded)

VIII. **PFFMAP: Exploitation of Particle Filters for Network-on-Chip Mapping**

BAYAR S., YURDAKUL A.

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, vol.23, no.10, pp.2116-2127, 2015 (SCI-Expanded)

IX. **A dynamically reconfigurable communication architecture for multicore embedded systems**

BAYAR S., YURDAKUL A.

JOURNAL OF SYSTEMS ARCHITECTURE, vol.58, pp.140-159, 2012 (SCI-Expanded)

## Articles Published in Other Journals

I. **FPGA Design of a High- Resolution FIR Band-Pass Filter by Using LabVIEW Environment**

TATAR G., BAYAR S., ÇİÇEK İ.

European Journal of Science and Technology, no.29, pp.273-277, 2021 (Peer-Reviewed Journal)

II. **FPGA Design of a Fourth Order Elliptic IIR Band-Pass Filter Using LabVIEW**

TATAR G., ÇİÇEK İ., BAYAR S.

European Journal of Science and Technology, vol.0, no.26, pp.122-127, 2021 (Peer-Reviewed Journal)

III. **Parallel Implementation of the GPR Techniques for Detecting and Mapping Ancient Buildings by Using CUDA**

Mumcu M. C., Bayar S.

European Journal of Science and Technology, pp.352-359, 2020 (Peer-Reviewed Journal)

IV. **A FAST AND ENERGY EFFICIENT PARALLEL IMAGE FILTERING IMPLEMENTATION ON RASPBERRY PI'S GPU**

POLAT A., BAYAR S.

European Journal of Technique, vol.10, no.2, pp.322-330, 2020 (Peer-Reviewed Journal)

V. **Gömülü Sistem Üzerinde Uygulanan İkili Yedekleme Yöntemi ile Aksaklığa Dayanıklı Yazılım Mimarisi**

SORKUN M. C., BAYAR S.

Deu Muhendislik Fakultesi Fen ve Muhendislik, vol.19, pp.63-70, 2017 (Peer-Reviewed Journal)

VI. **E-Defter ve E-Fatura Teknik Analizi: Örnek Bir Uygulama**

BAYAR S., Ülkar M. G.

Vergi Sorunları Dergisi, vol.38, pp.102-110, 2015 (Peer-Reviewed Journal)

## Refereed Congress / Symposium Publications in Proceedings

I. **Performance Evaluation of Real-Time Video Processing Edge Detection on Various Platforms**

TATAR G., BAYAR S., ÇİÇEK İ.

2023 IEEE 17th International Conference on Application of Information and Communication Technologies (AICT), 18 - 20 October 2023

II. **Hardware Acceleration of FIR Filter Implementation on ZYNQ SoC**

TATAR G., BAYAR S., ÇİÇEK İ.

IEEE 16th International Conference on Application of Information and Communication Technologies (AICT), Washington, Kiribati, 12 - 14 October 2022

III. **Performance Evaluation of Low-Precision Quantized LeNet and ConvNet Neural Networks**

TATAR G., BAYAR S., ÇİÇEK İ.

16th International Conference on INnovations in Intelligent SysTems and Applications (INISTA), Blarritz, France, 8 - 12 August 2022

- IV. **Performance Evaluation of Lightweight Cryptographic Algorithms on RISC-V**  
Mumcu M. C., ÇİÇEK İ., BAYAR S.  
IEEE 2022, 30th Signal Processing and Communications Applications Conference (SIU), Safranbolu, Turkey, 15 - 18 May 2022
- V. **Effect of Different Threshold Levels for Binarization Method in Image Classification**  
SAĞLAM S., BAYAR S.  
International Symposium on Fundamentals of Electrical Engineering 2020, Bucharest, Romania, 5 - 07 November 2020
- VI. **FPGA Based Fault Distance Detection and Positioning of Underground Energy Cable by Using GSM/GPRS**  
TATAR G., KILIÇ O., BAYAR S.  
International Symposium on Advanced Electrical and Communication Technologies ISAECT2019, Roma, Italy, 27 - 29 November 2019
- VII. **FPGA Implementation of CNN Algorithm for Detecting Malaria Diseased Blood Cells**  
SAĞLAM S., TAT F., BAYAR S.  
IEEE - International Symposium on Advanced Electrical and Communication Technologies, 27 - 29 November 2019
- VIII. **FPGA Based Step Motor Control For Solar Panels**  
TATAR G., BAYAR S., ALKAN M.  
The 13th IEEE International Conference, Application of Information and Communication Technologies, Baku, Azerbaijan, 23 - 25 October 2019
- IX. **Outlier Detection Based on Majority Voting: A Case Study on Real Estate Prices**  
Özçelik R., BAYAR S.  
12th International Conference on, Application of Information and Communication Technologies (AICT), Alma Ata, Kazakhstan, 17 - 19 October 2018
- X. **FPGA Implementation of 32-bit RISC-V Processor with Web-Based Assembler-Disassembler**  
GÜR E., Sataner Z. E., Durkaya Y. H., BAYAR S.  
International Symposium on Fundamentals of Electrical Engineering 2018, ISFEE 2018, Bükreş, Romania, 1 - 03 November 2018
- XI. **FPGA Based Bluetooth Controlled Land Vehicle**  
TATAR G., BAYAR S.  
International Symposium on Advanced Electrical and Communication Technologies (ISAECT), Rabat, Malta, 21 - 23 November 2018
- XII. **Performance analysis of e-Archive invoice processing on different embedded platforms**  
BAYAR S.  
2016 IEEE 10th International Conference on Application of Information and Communication Technologies (AICT), Baku, Azerbaijan, 12 - 14 October 2016
- XIII. **NoSQL Tabanlı, Odaklı İnternet Veri Toplama Servis Prototipi**  
Özbey C., BAYAR S.  
19. AKADEMİK BİLİŞİM KONFERANSI (AB2017), Aksaray, Turkey, 8 - 10 February 2017
- XIV. **Otomatik Ses Tanıma: Türkçe için Genel Dağarcıklı Akustik Model Oluşturulması ve Test Edilmesi**  
Özbey C., BAYAR S.  
19. AKADEMİK BİLİŞİM KONFERANSI (AB2017), Aksaray, Turkey, 8 - 10 February 2017
- XV. **An efficient mapping algorithm on 2-D mesh Network-on-Chip with reconfigurable switches**  
BAYAR S., YURDAKUL A.  
2016 International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS), İstanbul, Turkey, 12 - 14 April 2016
- XVI. **E-Defter Uygulamasında Özgün Adat Hesaplama Yazılımı**  
GÜR NALÇACI İ., BAYAR S.  
XVIII. AKADEMİK BİLİŞİM KONFERANSI, AB 2016, Aydın, Turkey, 30 January - 05 February 2016

- XVII. **A simple auditing mechanism for financial reports in e-Ledger project**  
CAMCI B., BAYAR S., ÜLKAR M. G.  
2015 9th International Conference on Application of Information and Communication Technologies (AICT), Rostov on Don, Russia, Russia, 14 - 16 October 2015
- XVIII. **Kullanıcı Tarafında eBelge Oluşturma ve Yazdırma Yazılım Deneyimleri**  
BAYAR S., ÜLKAR M. G., ŞEN M. A.  
Proceedings of the 9th Turkish National Software Engineering Symposium, İzmir, Turkey, 9 - 11 September 2015
- XIX. **E-Belge Uyum Yazılımı Deneyimleri**  
BAYAR S., ÜLKAR M. G., TERCAN Y.  
Proceedings of the 9th Turkish National Software Engineering Symposium, İzmir, Turkey, 9 - 11 September 2015
- XX. **E-Defter Finansal Raporlama Yazılımı ve Karşılaşılan Zorluklar.**  
BAYAR S., ÜLKAR M. G., KUZU R. S.  
XVII. AKADEMİK BİLİŞİM KONFERANSI, AB 2015, Turkey, 4 - 06 February 2015
- XXI. **Türkiyede ve Avrupada E-Fatura Uygulaması**  
BAYAR S., ÜLKAR M. G., DOĞAN U.  
XVII. AKADEMİK BİLİŞİM KONFERANSI, AB 2015, Turkey, 4 - 06 February 2015
- XXII. **E-Defter Mizan Raporu Uygulaması Geliştirme Deneyimleri**  
ÜLKAR M. G., BAYAR S.  
TBD 31. Ulusal Bilişim Kurultayı (Bilişim2014), Turkey, 6 - 09 November 2014
- XXIII. **E-Defter Uygulaması Kapsamında Çok Bileşenli Finansal Raporlama Yazılımı Geliştirme Deneyimleri**  
ÜLKAR M. G., BAYAR S.  
Proceedings of the 8th Turkish National Software Engineering Symposium, Turkey, 8 - 10 September 2014
- XXIV. **Efficient Implementations of Multi-pumped Multi-port Register Files in FPGAs**  
YANTIR H. E., BAYAR S., YURDAKUL A.  
2013 Euromicro Conference on Digital System Design, Los Alamitos, CA, USA, 4 - 06 September 2013
- XXV. **A self-reconfigurable platform for general purpose image processing systems on low-cost spartan-6 FPGAs**  
BAYAR S., TÜKEL M., YURDAKUL A.  
6th International Workshop on Reconfigurable Communication-Centric Systems-on-Chip (ReCoSoC), Montpellier, France, 20 - 22 June 2011
- XXVI. **Gömülü Çoklu İşlemcili Sistemlerde Yeniden Betimlenebilir Haberleşme Protokolleri**  
BAYAR S., YURDAKUL A.  
2. Gömülü Sistemler ve Uygulamaları Sempozyumu, Turkey, 4 - 05 November 2010
- XXVII. **Self-reconfiguration on Spartan-III FPGAs with compressed partial bitstreams via a parallel configuration access port cPCAP core**  
BAYAR S., YURDAKUL A.  
2008 Ph.D. Research in Microelectronics and Electronics, Istanbul, Turkey, 22 June - 25 April 2008
- XXVIII. **Dynamic Partial Self-Reconfiguration on Spartan-III FPGAs via a Parallel Configuration Access Port PCAP**  
BAYAR S., YURDAKUL A.  
2nd HiPEAC Workshop on Reconfigurable Computing, 27 - 29 January 2008
- XXIX. **Exploitation of Run-Time Partial Reconfiguration for Dynamic Power Management in Xilinx Spartan III-based Systems**  
PAULSSON K., HÜBNER M., BAYAR S., BECKER J.  
3rd International Workshop on Reconfigurable Communication-centric Systems-on-Chip, ReCoSoC 2007, 18 - 20 June 2007

## Supported Projects

Bayar S., Akan Ö. B., TUBITAK Project, TERAFEMTO - 5G MOBİL İLETİŞİM AĞLARI İÇİN TERAHERTZ FEMTOCELL, 2014 -

2017

Yurdakul A., TUBITAK Project, DEVELOPING AUTOMATION SOFTWARE FOR EMBEDDED SYSTEMS DESIGN, 2005 - 2010

## **Metrics**

Publication: 44

Citation (WoS): 30

Citation (Scopus): 91

H-Index (WoS): 4

H-Index (Scopus): 6

## **Non Academic Experience**

İdea Teknoloji Çözümleri Bilg. San. ve Tic. A.Ş.

İdea Teknoloji Çözümleri Bilg. San. ve Tic. A.Ş.

Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany

Molex Electronic Solution, Ettlingen, Germany

Mercedes Benz Daimler Chrysler, Rastatt, Germany

TEMO Soft-Hardware Consulting e.K., Karlsruhe, Germany